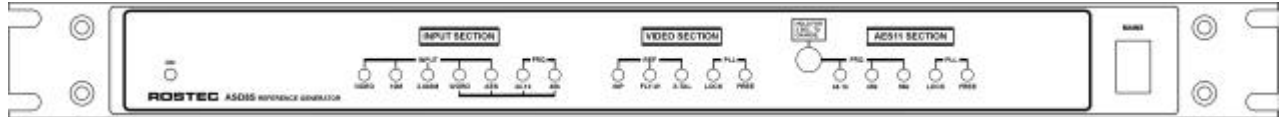


ROSTEC ASD8S

Digital Reference Generator
Rev.6, August 24 1999

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General description

The ASD8S is a crystal controlled AES grade1 reference generator with AES11, SDIF-2 Word and PAL composite video sync outputs.

It is able to lock on to standard PAL/CCIR or SECAM video, 10 MHz GPS, 2Mbit E1 G703, SDIF-2 Word or AES/EBU.

It is based upon an extensive sync safety philosophy, guarding efficiently against sync dropouts by means of a built in flywheel and a unique glide principle.

When an external reference is applied, the generator will slide gently into lock without any jumps or interruptions of the output sync signals.

When the external reference is momentarily absent or lost, the generator will immediately switch to internal flywheel mode, keeping the sync position and frequency inside narrow limits. When the external reference returns, the oscillator will slowly correct for the accumulated drift in time, gently bringing the outputs back into perfect sync. When the generator operates in flywheel mode, the flywheel inertia will gradually be exhausted and will eventually expire after a maximum of 40 seconds. If the incoming reference is not reestablished before this happens, control is handed over to the internal reference, which is of AES grade1 precision.

This scheme ensures continuous synchronization of the connected equipment, when large dropouts of the incoming sync signal is to be expected, and it will eliminate annoying "clicks" or frame jumps in the AES audio signal chain.

The phase locked loop exhibits an excellent Jitter Rejection Ratio, and is able to clean up and stabilize a jittery house sync, an important ability when the generator is connected to delicate or sensitive equipment.

When more than one input source is connected, the generator automatically selects the active input by priority: 1: Video. 2: 10M. 3: 2M. 4: Word. 5: AES. 6: Internal.

Powering up

There are no special considerations to observe when powering up the unit. Allow a warm up period of 5 minutes to let the internal oven crystal reference settle to its 1 ppm absolute frequency precision. If an external reference is connected to any of the generators inputs upon start up, the generator will immediately be able to achieve lock, as long as the incoming reference is better than +/-50 ppm in absolute frequency precision.

Front panel indication with no external reference connected

When there are no external references connected to the unit, it will operate on its own grade1 internal crystal reference. The input circuitry will be passive and all LEDs in the *Input Section* will be extinguished.

In the *Video Section* the X-TAL LED will light up, indicating the current choice of reference. The FREE LED will also light up, showing that the generator is not locked to any source (*Note that the internal reference is not a source, which the generator locks on to. It is a default idle state*).

The *AES Section* will indicate the chosen sampling frequency and indicate a PLL LOCK, showing that the AES generator circuit is locked to the Video circuit. The PLL LOCK/FREE should under normal operation always indicate LOCK. It can be considered a status indicator.

Front panel indication with external reference connected

When an external reference is connected to the unit, the corresponding LED will light up in the *Input Section*, indicating that the input has been accepted as a sync source. The *Video Section* will change to INP, and after 1 to 6 seconds the Video generator circuit will achieve lock and the LOCK LED will light up. The *AES Section* will

remain unchanged, as the AES generator circuit constantly tracks the Video generator circuit. When the external input is removed or for some reason lost, the corresponding LED in the *Input Section* will extinguish, and the *Video Section* will immediately change to FLY-W reference and FREE will light up. In this state the generator operates on its internal flywheel circuit, and it will continue to do so until either the flywheel inertia is exhausted or the reference is reestablished, at which point normal locked operation is resumed. The Word and AES input circuit will autodetect incoming sampling frequency, indicating this on the 44.1 kHz or 48 kHz LED in the *Input Section*. However, when the AES input receives a signal at 44.1 kHz sampling frequency, the generator automatically switches to WORD mode, due to the lack of a useful relationship between the AES block structure and the PAL video frame at this frequency (see *relationship between Video, Word and AES*).

Front panel control buttons

The Video input circuit has two distinct modes, jump-mode and glide-mode. Switching between these two modes is done automatically, based upon measuring the time distance between the position of the incoming video sync and output video sync. The default is glide-mode, but if the measured time difference is greater than 5 lines, the input circuit switches to jump-mode. The first received video frame pulse will then force the video sync output to jump to the input sync position with less than one video line in time difference. The input then switches to glide-mode and gently pulls the input and output into perfect sync. When the external video signal is removed or applied while in glide-mode (which is the normal mode), the generator will slide gently between flywheel mode and lock without any jumps or interruption of the output sync signal.

Note that the AES section can be set by internal jumpers to perform the same jump, or it can be set to catch up by "gliding" after the Video section. Gliding may take 30 seconds worst case, during which PLL FREE in the AES section will light up.

The switch in the *AES Section* changes the output sampling frequency for the Word and the AES outputs. It toggles between the three available sampling frequencies, and it is protected against accidental use by a 2 seconds time delay. At first this is annoying, but it is a necessary precaution. Changing the sampling frequency in a synchronized environment is a serious thing.

Back panel, Video input

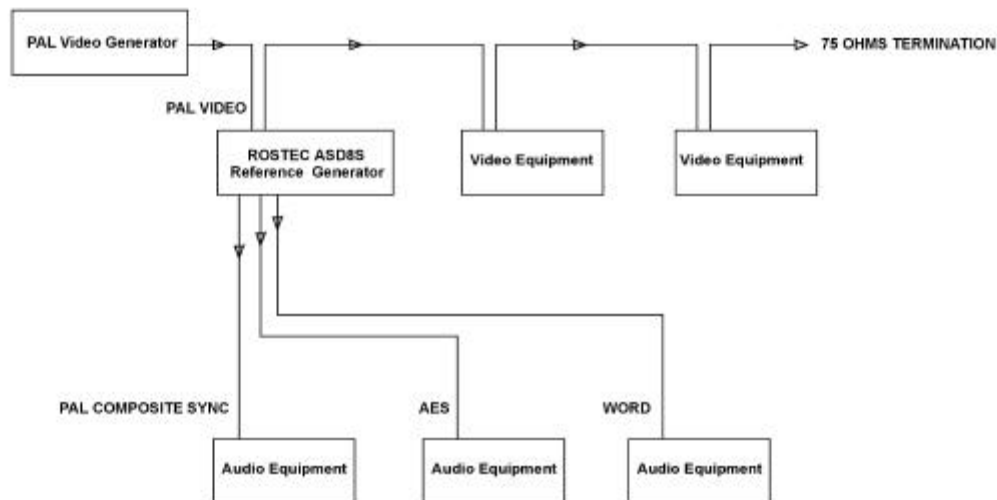
The Video input connectors are the standard BNC types, and the signal is linked directly between them. The input is not terminated internally; its impedance is 1 kohms. This makes it possible to connect the generator in a serial chain with other equipment and placing the correct 75 ohms termination at the end of the chain.

The input will accept standard negative going PAL/SECAM video or composite video sync with amplitudes ranging from 0.1 to 4.0V peak to peak.

The switch on the back panel switches the video input between balanced and unbalanced mode. The normal mode is unbalanced.

The balanced mode is used when ground loops are present in the installation. The ground is lifted and connected to the inverting input of the input buffer, thus creating a balanced configuration with the screen of the input cable as the inverting input and the core as the non-inverting input.

Care should be taken not to exceed the Common Mode Range of the input circuit, which is 3.0 V.



A note on video

The ASD8S will lock to standard interlaced PAL video, 625 lines, 50 Hz vertical frequency and 15625 Hz horizontal frequency. The video signal must be interlaced, as the input sync separator extracts timing information from the odd/even video field information in the composite sync signal. Chrominance and 4.43 MHz subcarrier are not necessary.

Note that many low priced test bench video generators run in non-interlaced mode. This mode skips one horizontal line at the end of every odd/even field, thus in effect creating a 624 line full picture with identical odd/even fields. The horizontal frequency stays the same at 15625 Hz, but the vertical frequency is increased by 1600 ppm. This has absolutely no effect on standard monitors, television sets or VCRs as their capture range often exceeds 10%. But the ASD8S will not accept this signal as a sync source.

Also connecting a video source with the correct horizontal and vertical frequencies, but without odd/even field information, will not activate the input logic and the generator will not initiate a lock on sequence.

Back panel, 10M and 2.048M inputs

The 10MHz and 2.048MHz inputs are internally connected in the same way as the Video input, hardwired between the two input connectors for serial chain connection.

They are both unterminated and unbalanced. However, when the E1 G703 decoder board is fitted, the 2.048MHz input is transformer balanced

Back panel, Word input

The Word input uses a single BNC connector and it is TTL compatible, unterminated.

Back panel AES input

The AES input uses a standard 3-pole XLR female connector and is transformer balanced, 110 ohms terminated as prescribed in the AES/EBU standards for professional/broadcast equipment.

Back panel, Video Sync output

The Video Sync output uses standard BNC connectors. There are four individually buffered outputs, 75 ohms 300mV when terminated. The output format is PAL Composite Sync, black level, no 4.43 MHz subcarrier (colorburst) and no chrominance information.

Back panel, Word output

The Word outputs use standard BNC connectors. There are four individually buffered outputs, 75 ohms, TTL level.

Back panel, AES output

The AES outputs use standard 3-pole XLR male connectors. There are four individually buffered outputs, 110 ohms RS422 as prescribed in the AES/EBU standards for professional/broadcast equipment.

Back panel, AUX outputs

The AUX1 and AUX2 outputs use standard BNC connectors. These outputs can be configured to bring out various internally generated signals for use in the laboratory or on the test bench. There are two individually buffered outputs, 50 Ohms, TTL level.

Back panel, alarm relay

The alarm output uses a standard 4-pole XLR male connector, wired directly to a floating changeover relay. The relay changes state when incoming sync is lost or reestablished.

Pin 3 (the relay viper) and pin 2 is connected when input sync is present. Pin 3 and pin 4 is connected when incoming sync is absent. This provides a useful No Sync Alarm with an immediate warning in case the incoming sync drops away, giving the user the necessary time to correct the fault before timeout of the flywheel will happen.

It also will reveal an erratic sync source, which normally may not be reflected on the generators outputs, because the flywheel and glide function will work together to even out the missing periods.

Ability to reject jitter

The maximum permissible sample-to-sample jitter at the AES, 10M or 2M input is 45 nSec PP, equal to or less than one half cycle of the master clock.

The Video and Word inputs are more tolerant, and will accept and lock to input signals with up to 1 uSec of jitter.

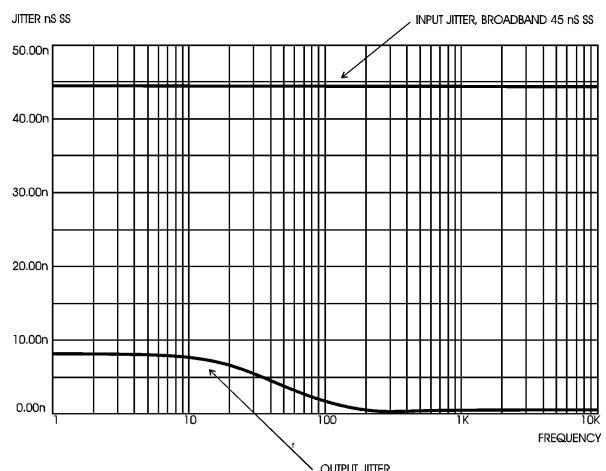
The jitter presented at the inputs will not directly be transferred to the outputs. It will be greatly reduced and in most situations almost total eliminated.

The curve below illustrates the excellent Jitter Rejection Ratio of the ASD8S. With 45 nSec broadband jitter superimposed on the AES input signal, the measured jitter at the AES output is plotted against frequency.

The corner frequency of the jitter rejection curve is approx. 23 Hz. In the frequency band, where excess jitter can create problems in standard A/D and D/A converters, the output jitter is reduced to 1 nSec at 700 Hz, fading to less than 400 pSec at higher frequencies (residual HCMOS buffer noise)

45 nSec of broadband jitter is a rather extreme case. Even a poorly designed studio environment should not create more than 10-15 nSec of jitter, typically at frequencies above 100 kHz.

The ASD8S will in a real world situation totally ignore that kind of jitter.



ASD8S Jitter rejection curve.
Input: AES Output: AES

Additional Technical Information

General

The ASD8S has a straight forward, yet much more powerful architecture than its predecessor, the ASD6. The input reference is automatically selected by priority from left to right on the front panel and fed to the Video section, which always acts as a master for the AES section. The AES generator always locks the Z-preamble (at 48 and 96 kHz) or the X-preamble (at 44.1 kHz) to the video frame start, no matter which reference the video generator is locked to. The internal flywheel is able to keep the video running at better than 0.2 ppm accuracy for up to 40 seconds, in case the incoming sync is momentarily absent.

Video input cct

The Video generator circuit locks the input video frame to the output video frame by slowly changing the frequency of the crystal oscillator. The maximum time shift between input and output during the lock on sequence is $\frac{1}{2}$ video frame, equal to 10 mSec. A time difference of more than 5 lines (approx 300 uSec) will activate a time jump, after which the lock time will be less than 10 seconds.

10 MHz input cct

The 10 MHz input is intended for use with GPS receivers. There is no position information in 10 MHz signal, so the video generator locks the leading edge of the video frame to the leading edge of the incoming square wave. When the input is lost and reestablished, the generator simply grabs the first available leading edge of the 10 MHz signal and locks the leading edge of the video frame to it.

The circuit evaluates the incoming signal for errors and continuity for 2 seconds before it locks on to it. The lock time is approximately 3 seconds and the maximum time shift between input and output during the lock on sequence is 200 nSec. This is equal to an output frequency correction of less than 1 ppm.

2.048 MHz input cct

The 2.048 is in principle identical to the 10 MHz input, but the lock time is slightly longer. The lock time is approximately 5 seconds and the maximum time shift between input and output during the lock on sequence is 500 nSec. This is equal to an output frequency correction of less than 1 ppm.

An optional decoder board for the 2Mbit E1 CCIT G703 line is available. The board has a transformer balanced E1 line receiver interface, which performs clock recovery and jitter attenuation. The jitter attenuator is based on a crystal controlled reference clock, able to phase lock to the recovered clock.

This scheme dramatically reduces incoming jitter, which often is substantial on an E1 line.

The output circuit exhibits excellent output clock stability, and the receiver has a jitter tolerance exceeding the requirements of Publications 43802, 43801, 62411 amended, TR-TSY-000170 and CCITT REC G.823

The recovered clock is evaluated for errors and continuity for 2 seconds, after which it is routed to the normal 2.048 MHz input circuit. Lock time and time shift parameters are identical to normal 2.048 MHz operation.

Loss of signal is detected upon receiving 175 consecutive zeroes, after which frequency control immediately is handed over to the main flywheel circuit. The signal is accepted again when ones density reaches 12,5%, based on 175 bits periods with less than 100 consecutive zeroes, as is prescribed in ANSI T1.231-1993.

Word input cct

The Word signal contains only left/right position information (X/Y preamble) so the video generator locks the start of the video frame to the leading edge of the incoming square wave. The mechanism is the same as used by the 10 MHz and 2.048 MHz inputs, but the maximum time shift during the lock on sequence is 11.3 uSec and the lock time is approximately 8 seconds. The maximum frequency correction will be equal to the VCO maximum frequency deviation, which is 100 ppm.

The incoming sampling frequency is automatically detected and indicated on the front panel LEDs.

AES input cct

When the incoming sampling frequency is 48 kHz, the video generator uses the Channel Block Start information in the signal to lock the Z-preamble to the video frame start.

There are 5 AES blocks for every video field and the maximum time shift during lock on is $\frac{1}{2}$ block equal to 2 mSec.

The maximum frequency correction will be equal to the VCO maximum frequency deviation, which is 100 ppm.

When the incoming sampling frequency is 44.1 kHz, the generator switches to word mode, due to the lack of useful relationship between the AES blocks and the video field at this frequency.

(The word/field relationship at 44.1 kHz is 882/1 but there are still 192 words pr. AES block, which continuously places the block start at a different position in the video frame).

The incoming sampling frequency is automatically detected and indicated on the front panel LEDs.

Flywheel circuit

When the input is lost, an internal flywheel circuit immediately takes over, keeping both clock frequency and position of the preambles inside narrow limits. When the input returns, the generator slowly corrects for the accumulated drift in time, gently bringing the preambles back into perfect sync.

When operating in flywheel mode, the flywheel inertia will gradually be exhausted and it will eventually expire after a maximum of 40 seconds. If the input is not reestablished before timeout, clock control is handed over to the internal crystal reference.

There are jumpers for 2.5, 5, 10, 20 and 40 seconds of flywheel time. Operation of the flywheel circuit is identical in all input modes.

Video LOCK/FREE indicators

The LOCK LED indicates that the video is locked to incoming sync. When flywheel or internal crystal reference is selected, the FREE LED will light up. Also when the generator is searching for lock, FREE lights up until at phase lock is achieved. If FREE stays on longer than expected (see the various lock times) it indicates that the incoming sync is invalid or outside the capture range of the generator. Capture range follows the

maximum frequency deviation, i.e. equal to 100 ppm.

AES LOCK/FREE indicators

The LOCK LED should always be on during normal operation. FREE will light up from 5 to 20 seconds when output sampling frequency is changed or when a video jump is performed, indicating that the AES generator is catching up on the video generator.

44.1kHz/48kHz/96 kHz sampling frequency

The AES/Word generators output sampling frequency is selected by a pushbutton on the front panel, toggling between the available frequencies. The pushbutton has a 2 seconds time delay to protect against accidental change. Note that the output sampling frequency can be chosen independently of the input sampling frequency. Default start up sampling frequency can be set by internal jumpers to 44.1 kHz, 48 kHz or 96 kHz.

Video Sync Outputs

The video sync outputs are available on four BNC connectors on the back panel. The outputs are individually buffered, 75 ohms and 300 mV when terminated according to the PAL/CCIR Video standard.

The output signal is PAL B/G 625 line interlaced composite sync, video black level, no 4.43 MHz subcarrier (colorburst) and no chrominance information. The signal is intended for use with digital audio equipment, which has no use of these signals.

Keeping the HF content out of the sync signal reduces the possibility of producing jitter in the sync input circuit in audio equipment, which often use standard video sync separators and input circuits with little or poor HF screening.

Word Outputs

The Word outputs are available on four BNC connectors on the back panel. The outputs are individually buffered, 75 ohms and TTL level.

The word output frequency follows the chosen sampling frequency on the front panel, i.e. 44,1 kHz, 48 kHz or 96 kHz.

The rising edge of the word is aligned to the AES subframe A and the trailing edge is aligned to the subframe B. Thus a high level indicates left channel and a low level indicates right channel of the audio data.

AES Outputs

The AES outputs are available on four XLR connectors on the back panel. The outputs are individually buffered, 110 ohms, transformer balanced and 4V PP when terminated.

The AES signal is intended for synchronization purposes and should normally be empty of audio data, i.e. all audio data bits are set to zero. This minimizes the build-up of clock jitter in the connected cable, because the format produces a biphase coded AES signal with a large portion of the frame having identical pulses.

However, some commercially available AES receiver chips exhibits PLL lock problems when subjected to a "black" AES signal, producing an unstable and jittery master clock.

The problem can be overcome by setting the first eight audio data bits to 1 and the remaining sixteen bits to 0. This gives a DC offset in the

audio signal of -90 dBFS or approximately 0.2 mV with reference to +18 dBu.

A standard digital audio input circuit will easily accommodate this DC offset, and the scheme efficiently eliminates the problem.

AUX1 and AUX2 Outputs

The AUX outputs are configurable outputs. A range of internally generated signals can be brought out on the BNC connectors by setting jumpers on the main board.

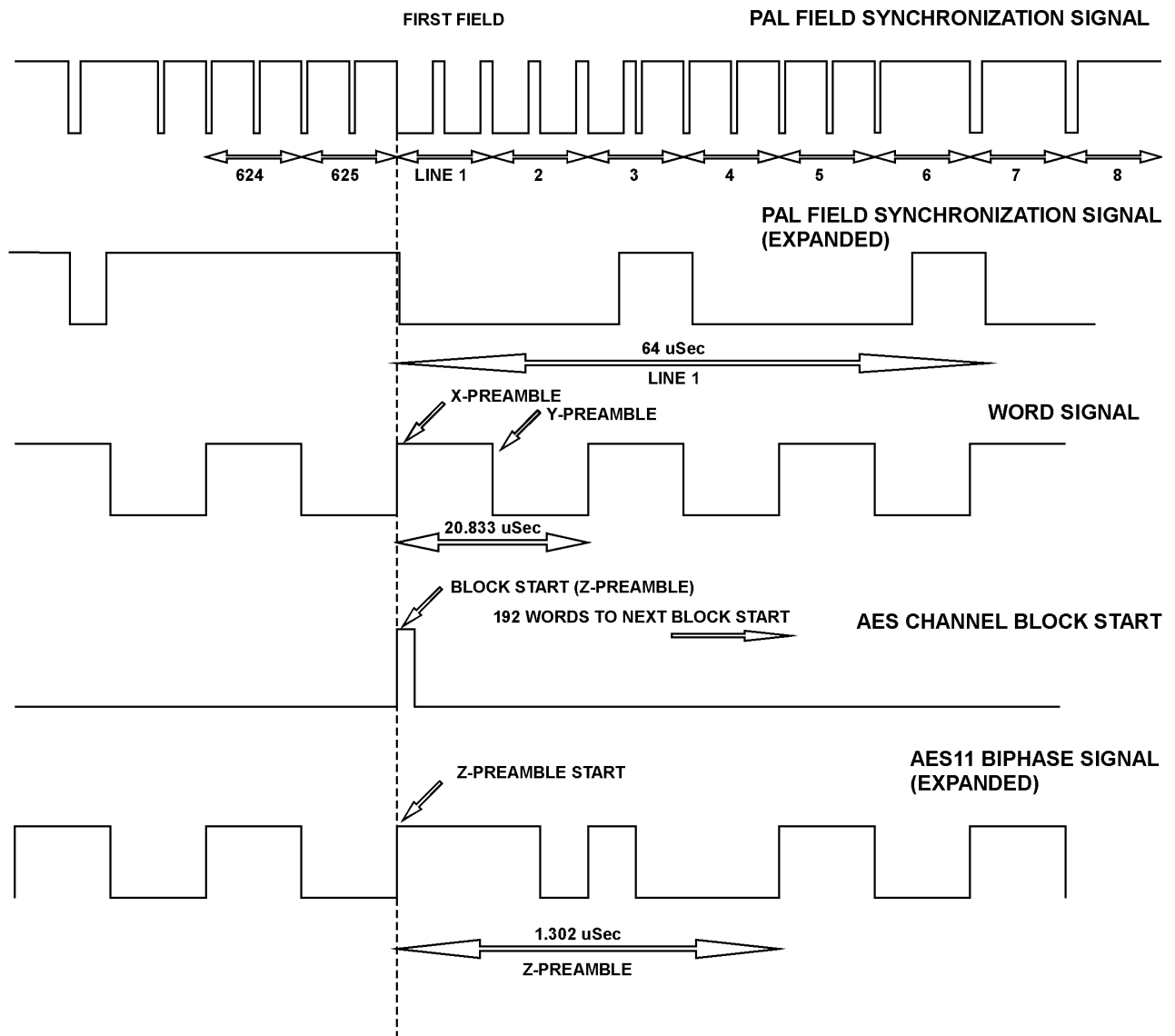
AUX1 can be configured to:

- Z-preamble
- X-preamble
- 2 x word
- 64 x word
- 128 x word
- 256 x word

AUX2 can be configured to follow AUX1 or to follow the signal on an open solder pad on the PCB. This pad can then be connected to various point of interest on the main board.

2 independent TTL compatible 50 ohms output buffers are available for this purpose.

Relationship between Video, Word and AES



The generator places the video field start, word start and AES block start as seen on the graphic representation above.

At 48 kHz sampling frequency, the relationship is straightforward, when it comes to synchronization.

1 Video field = 5 channel blocks = 960 words

1 channel block = 192 words

At 44.1 kHz sampling frequency, the relationship is less useful

1 video field = 882 words

But the AES block is still 192 words, so no simple defined position of the AES block start in the video field is possible.

Mechanical and electrical specifications:

Dimensions : Width 19 inch , height 1U (44 mm), depth 320 mm

Weight : 5,5 kg

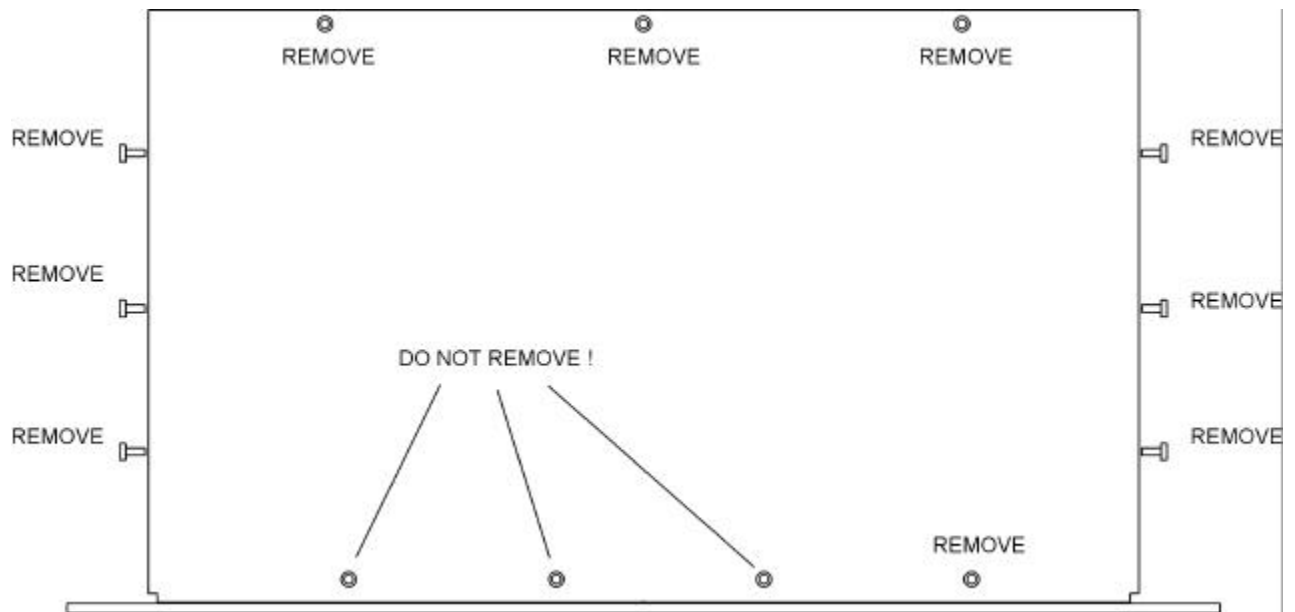
Power requirements : 180 - 240 VAC 50 Hz, 8 Watts

Reference Inputs : Composite PAL Video, balanced 1kohm, 0,1 -4,0V PP
: AES balanced 110 ohms RS422
: SDIF-2 word clock, 10 kohms, TTL level
: 10 MHz clock, 10 kohms, TTL level
: 2.048 MHz clock, 10 kohms, TTL level
: Optional 2Mbit E1 CCITT G703 transformer balanced input, 1kohm.

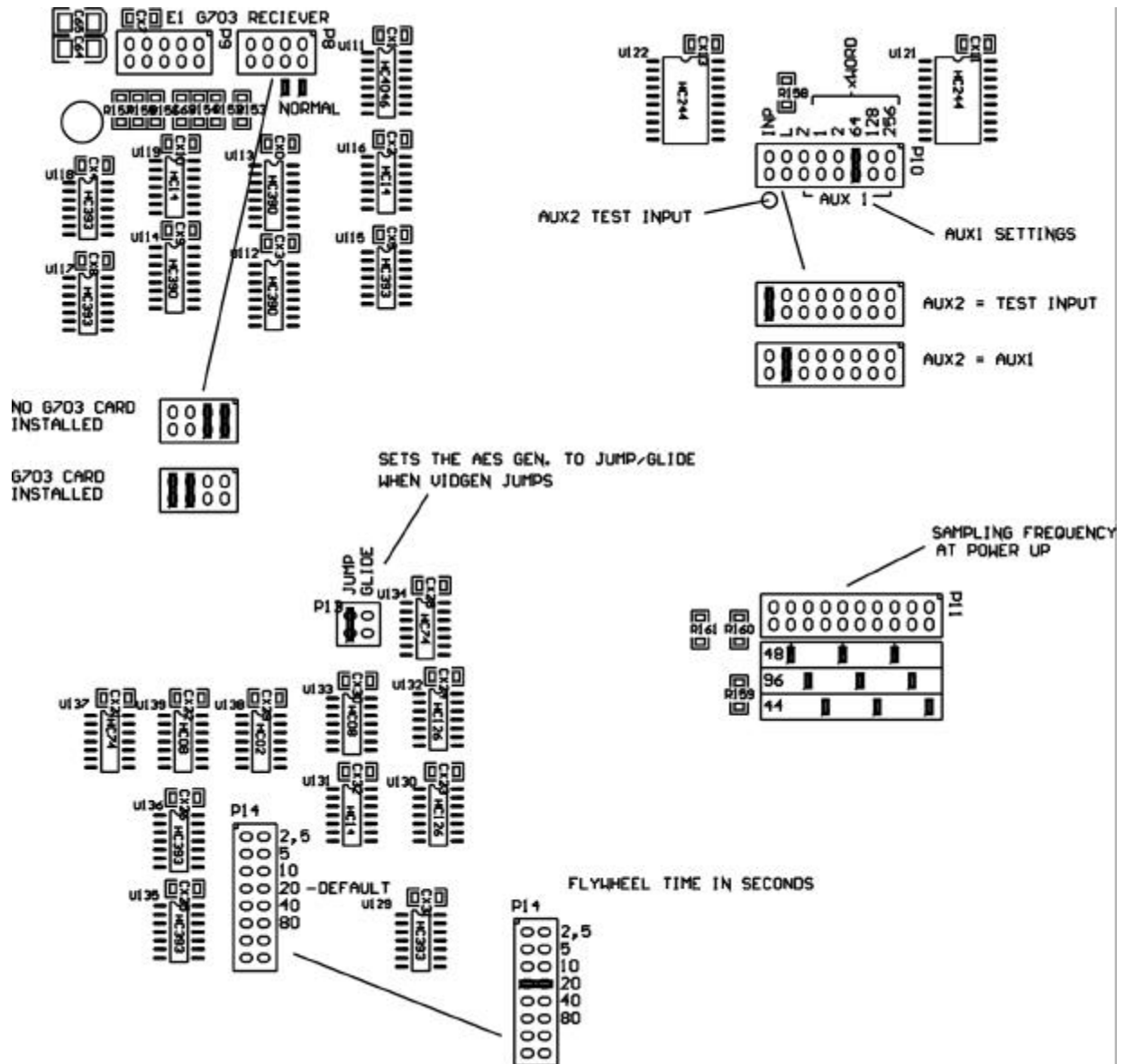
Outputs : Composite PAL video sync, black level.
75 ohm, 0,3V PP terminated
: AES11 transformer balanced 110 ohms RS422
: SDIF-2 word clock, 75 ohm, TTL level
: AUX output, configurable, 50 ohm, TTL level
: No-sync alarm relay, SPDT 100V 0.5A

Stability/accuracy : Oven crystal accuracy 1 ppm/25 deg. C, stability 0.5 ppm 0/+50 deg. C
: PLL capture range max. +/-100 ppm.
: PLL jitter < 1 nSec SS, 700Hz - 100kHz

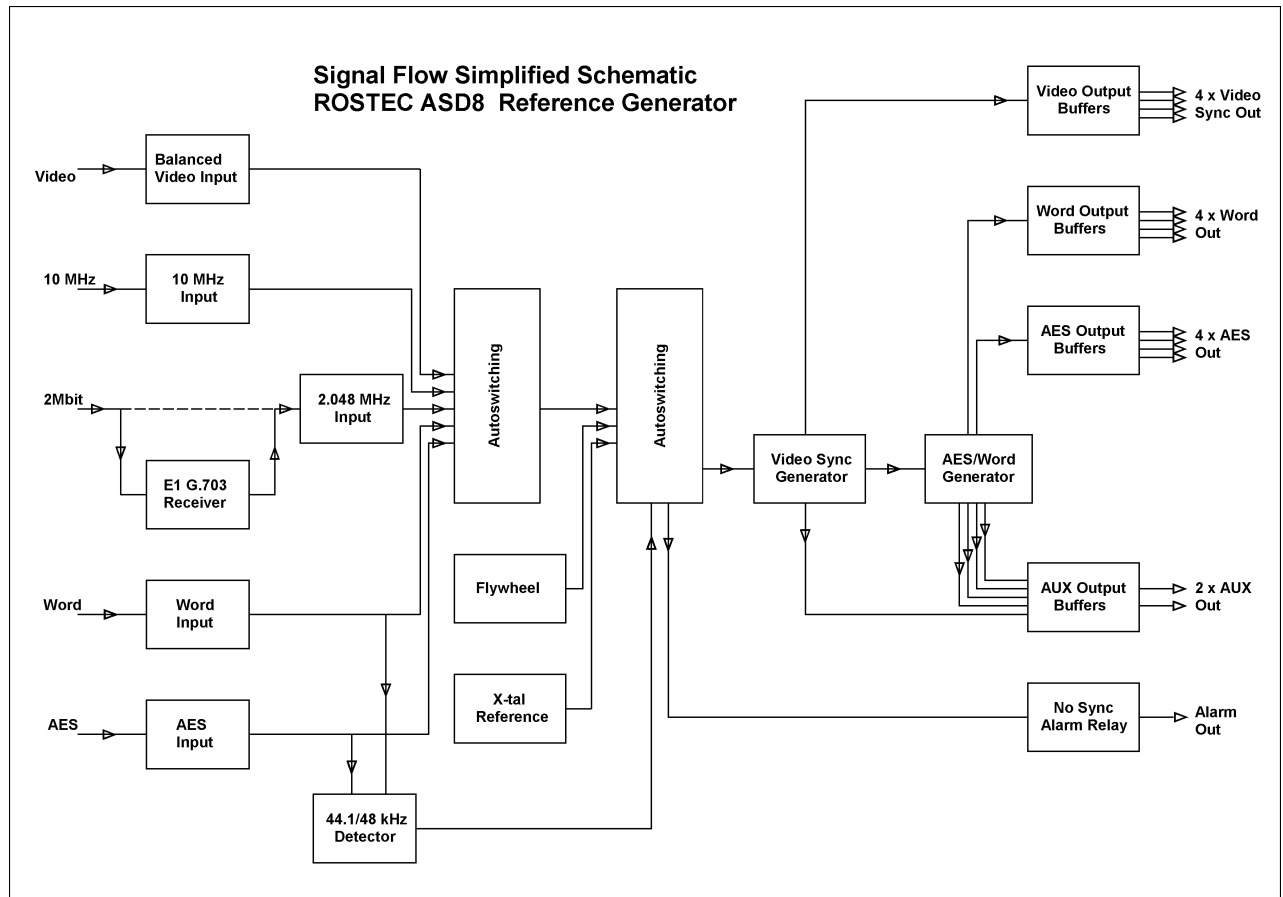
Taking the lid off:



Jumper setting PCB Main Board Rev. 6



Block schematic



Circuit Schematics:

(Available upon request)